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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,360	02/12/2001	Dae Young Kim	2950-0186P	7013

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EXAMINER
BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/780,360	KIM ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 February 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-7 are presented for examination.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

In the "Brief Description of the Drawings" section, the description of Figure 1 should contain the words "Prior Art".

The term ESM-modulation (page 2 line 14) is not defined. For the purpose of examination, the examiner will assume a modulation system that converts one byte (8 bits) into 16 channel bits and does not require merging bits for suppressing DC components (Eight to Sixteen Modulation).

On the abstract page (10), the title should be "Abstract" not "Abstract of Disklosure"

Appropriate correction is required.

Allowable Subject Matter

Claims 2-4 and 6-7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Massoudi, U.S. Patent No. 6,363,511.

As per claims 1 and 5, Massoudi teaches a device, method, and system for detecting and correcting errors in ECC block data as it is read sequentially from a DVD medium. In one embodiment, a device for detecting and correcting errors in error

correction coded (ECC) data blocks are read sequentially from a DVD medium. Each ECC data block is defined as a two dimensional block of a plurality of columns and rows. Each of the ECC data blocks is read from the DVD medium sequentially in rows. The device includes row correction circuitry, a buffer, column correction circuitry, and repeat correction circuitry. The row correction circuitry is configured to sequentially receive the rows of an ECC data block for detecting and correcting up to a first predetermined number of errors in each of the received rows. The buffer is coupled to the row correction circuitry for receiving the error corrected rows of the ECC data block as a receiving buffer. The buffer also stores the ECC data block as a correction buffer when all the rows of the ECC data block have received. The column correction circuitry is coupled to the row correction circuitry and the buffer to sequentially receive the row error corrected rows of the ECC data block for detecting the uncorrected errors. The column correction circuitry is also configured to correct the uncorrected errors in the columns of the ECC data block that is stored in the correction buffer. The repeat correction circuitry is coupled to the buffer for detecting and correcting the remaining uncorrected errors in the correction buffer. In another embodiment, a method for detecting and correcting errors in ECC data blocks, each of which comprising a plurality if rows and columns. The method sequentially receives the rows of an ECC data block. Then, the method detects errors in each of the received rows of the ECC data block and corrects up to a first predetermined number of the errors in each of the rows in the ECC data block. Each of the corrected rows is then stored in a storage unit. While storing the corrected rows, the method of the present invention receives each of the corrected

rows sequentially for detecting the uncorrected errors in the columns of the ECC data block. The method then corrects the uncorrected errors in the columns of the ECC data block when all the rows of the ECC data block has been stored. Another embodiment, includes a receiving means, a row error detecting means, a row error correcting means, a storing means, a column error detecting means, and a column error correcting means. The receiving means sequentially receives the rows of an ECC data block. The row error detecting means detects errors in each of the received rows of the ECC data block and the row error correcting means corrects up to a first predetermined number of the errors in each of the rows in the ECC data block. The storing means stores each of the corrected rows. The column error detecting means receives each of the corrected rows sequentially and detects the uncorrected errors in the columns of the ECC data block while each of the corrected rows are being stored. The column error correcting means corrects the uncorrected errors in the columns of the ECC data block when all the rows of the ECC data block have been stored. This provides a device and method that can detect and correct errors in the rows of an ECC block data without waiting for an entire ECC block to be assembled in a buffer. Furthermore, the device and method of the present invention performs column corrections, and repeat corrections if necessary, as soon as all the rows of the ECC block have been received. (Column 3 line 63 through column 4 line 67) Figures 2A-2C show the standard DVD sector with the inner and outer parity appended to the rows and columns as also described in the present application on pages 1 and 2 of the disclosure.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,901,157 Hogan

This patent teaches a multi-level error correction device and method that significantly improves access time of current technology storage systems while providing reliable multi-level error correction. As such, it is suitable for use when the error correction codes within a unit block are interleaved. This invention is able to achieve improved access performance by calculating the "contribution" to the outer error correction code (ECC2) fields for the unit block of both the old sector to be changed and new replacement sector. The contribution due to the old is removed from the original ECC2 and that of the new is added to the original ECC2. For one embodiment, calculation of the ECC2 contribution is accomplished by a matrix multiplication. The elements of the matrix are determined by which sector of the unit block is to be changed. Removing or adding a contribution to the original ECC2 is accomplished by a simple exclusive or process. An alternative way of calculating the contribution to ECC2 of the sector is to accumulate the contribution while reading the original block. This is calculated in the same manner as is the normal ECC2, but zeros are substituted for all data bytes other than those of the sector to be changed.

U.S. Patent No. 6,430,723 Kodama et al.

This patent teaches an error correcting device that includes a receiving circuit for receiving data in a unit of block, an error correcting circuit for detecting an error in the data received by the receiving circuit and correcting the error, a transmission circuit for transmitting the data whose error has been corrected by the error correcting circuit, and a storage device having two areas each having a storage capacity corresponding to at least one block of the data. The transmission circuit reads the data corrected by the error correcting circuit from one of the areas of the storage device, and simultaneously, the receiving circuit writes the received data into said one area of the storage device at an address where the transmission circuit has already read out the error-corrected data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cynthia Britt
Examiner
Art Unit 2133

CHB
July 6, 2003

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100